

# Development of a Silicon Tracker for the All-sky Medium Energy Gamma-ray Observatory Prototype

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**Abstract**—The gamma-ray sky from several hundred keV to  $\sim$  a hundred MeV has remained largely unexplored due to the challenging nature of detecting gamma rays in this regime. At lower energies, Compton scattering is the dominant interaction process whereas at higher energies pair production dominates, with a crossover at a few MeV. Thus, an instrument designed to work in this energy range must be optimized for both Compton and pair-production events. *AMEGO*, the All-sky Medium Energy Gamma-ray Observatory, a Probe-class mission in consideration for the 2020 decadal survey, is designed to operate at energies from  $\sim 200$  keV to  $> 10$  GeV with over an order of magnitude increase in sensitivity and with superior angular and energy resolution compared to previous instruments. *AMEGO* comprises four major subsystems: a plastic anti-coincidence detector for rejecting cosmic-ray events, a silicon tracker for tracking pair-production products and tracking and measuring the energies of Compton-scattered electrons, a cadmium-zinc-telluride (CZT) calorimeter for measuring the energy and location of Compton scattered photons, and a CsI calorimeter for measuring the energy of the pair-production products at high energies. A prototype instrument, known as *ComPair*, is under development at NASA's Goddard Space Flight Center and the US Naval Research Laboratory. In this contribution, we provide details on the development of the silicon tracker subsystem.

**Index Terms**—gamma-ray, instrumentation, future missions, AMEGO

## I. CONTEXT

To date, the region of the electromagnetic spectrum between 100 keV and 100 MeV has had very limited astrophysical observations. One of the difficulties in constructing an instrument to operate at these energies is that around a few hundred keV, gamma-ray interactions are dominated by Compton scattering, and at higher energies  $e^+e^-$  pair production is the dominant process, with a crossover

at a few MeV. An instrument designed to work in this energy regime must thus be optimized for both Compton and pair-production events; several designs have been proposed in the past to accomplish this (e.g. [1], [2]). *AMEGO* is a NASA-led Probe-class mission concept being submitted to the 2020 Decadal Survey. *AMEGO* will provide an order-of-magnitude increase in sensitivity above previous measurements made in the MeV band (see Figure 1), will be sensitive to polarization, and will have sufficiently high energy resolution for spectroscopic measurements of nuclear emission lines. An overview of the instrument design and simulated performance can be found in Refs. [3] and [4], respectively.

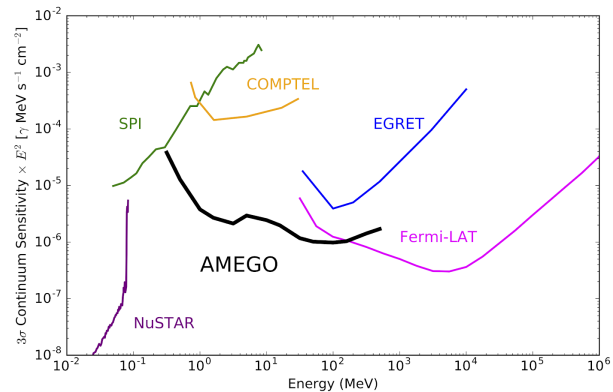


Fig. 1. *AMEGO* will provide over an order-of-magnitude increase in sensitivity over other instruments in the MeV band [4].

A schematic of the hardware design is given in Figure 2. *AMEGO* comprises four major subsystems: a plastic anticoincidence detector for vetoing cosmic-ray events, a silicon tracker system for measuring particle tracks and energy deposition (the subject of this work), a cadmium-zinc-telluride (CZT) calorimeter for measuring the direction and energy of Compton scattered photons [5], and a CsI

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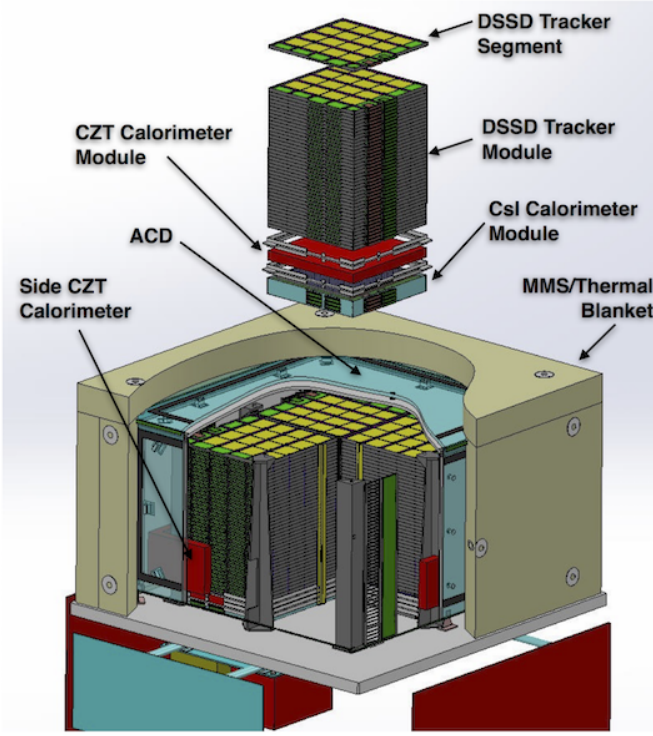


Fig. 2. Hardware design for *AMEGO* [3].

calorimeter for measuring the position and energy of pair-production events [6].

## II. THE SILICON TRACKER SUBSYSTEM

### A. Design

The *AMEGO* tracker comprises 60 layers of double-sided silicon strip detectors (DSSDs) vertically separated by 1 cm connected in a  $4 \times 4$  configuration, referred to as a “tower”. In the current design, each detector is a 9.5 cm square, 500  $\mu\text{m}$  thick with a strip pitch of 500  $\mu\text{m}$ , yielding 192 strips per side. These parameters, in addition to the vertical spacing between layers (1 cm) dictate the angular resolution, field of view, and collection area of the telescope. The detector readout electronics are located along two edges of each segment (one for each the  $x$  and  $y$  directions) with a minimal amount of passive material between detector elements. The full *AMEGO* tracker has four identical towers; this modular design simplifies integration and allows for the easy production of spare components. Furthermore, this helps minimize the amount of passive material within the instrument, which is crucial to

operation in the Compton regime. ASICs are used to read out the strips; the ASICs provide pulse-height information which is required to measure the energy of the Compton recoil electron, for measuring the energy of the particles in low-energy pair-production events, and for identifying pair-production particle tracks for event reconstruction.

A prototype instrument, known as *ComPair* (Compton/Pair-Production), is currently being developed at NASA Goddard and the Naval Research Laboratory. The prototype will include small versions of each of the four *AMEGO* subsystems and has an ultimate goal of flying as a balloon payload. When fully assembled, the prototype tracker will comprise 6-10 single-detector layers; the development of this subsystem is discussed in the following sections.

### B. Detector Development

A number of DSSDs have been purchased from Micron Semiconductor [7] and are currently being fabricated; several test units have arrived at Goddard and are currently undergoing characterization and testing. Each detector is a 10 cm square and 500  $\mu\text{m}$  thick, with 192 strips per side, each with a pitch and width of  $\sim 510 \mu\text{m}$  and 60  $\mu\text{m}$ , respectively.

The first few silicon detectors will be thoroughly characterized and tested: bulk current-versus-voltage (IV) and capacitance-vs-voltage (CV) measurements will be made of each detector, and single strip measurements of components such as the bias resistors and coupling capacitors will be made and compared against measurements provided by Micron. This testing protocol is expected to be very time consuming (up to two weeks per detector); thus results from the first few wafers will define the testing strategy for subsequent wafers. It is likely that subsequent silicon wafers will be “bulk tested”; by combining signals of  $N$  strips while testing, the testing time is reduced by a factor of  $\sim N$ . Thus, every strip is still tested but the process is far less time consuming; this is important since when fully assembled, *AMEGO* would have some 370 thousand strips, making it impractical to test every single one. Using this method, the general vicinity of bad strips can be identified by comparing signals from bulk-tested strips with expected signals based on the single-channel results made on another detector.

Single-detector “carriers” have been designed to encapsulate and provide an interface to both sides

of the detectors (required for both biasing and readout). A CAD image of the carrier design is given in Figure 3 alongside a photo of a populated carrier. Each assembly uses two identical printed wire boards, with one flipped and rotated 90° to read out the orthogonal strips. The signals from the DSSDs are captured using elastomer connectors between the carrier boards and the detector, with a plastic spacer and base plate to provide rigidity. This design does not require any wire-bonding and allows detectors to be removed from the carriers if need be. Connectors are located on all four sides of the carrier and allow for multiple carriers to be connected (thus daisy-chaining the DSSDs) in both the  $x$  and  $y$  directions. The same connectors are used to interface with custom readout boards which contain ASICs and an FPGA for handling triggering (internal and external) and the readout of the individual ASICs.

Finally, performance measurements of a daisy-chained DSSD ladder will be made to quantify the total parasitic capacitance and provide insight into the performance of a large DSSD array in preparations for the full *AMEGO* design. The instrument must minimize the total amount of passive material within it; this is particularly important in the Compton regime where measuring the energy of the scattered electron is critical to event reconstruction. Due to total number of readout channels, using smaller detector arrays (e.g.  $2 \times 2$  detector ladders) is also impractical. Thus, understanding the noise performance of a large DSSD ladder is crucial to the development of a future Compton/pair-production telescope.

When daisy-chained, the capacitance of each DSSD adds linearly and the readout noise scales linearly with load capacitance (this is demonstrated in the next section), so a ladder will have significantly higher noise than a single detector. These measurements will be accomplished by daisy-chaining detectors into an “L-shape” with four detectors to a side (requiring seven total), mimicking a full  $4 \times 4$  *AMEGO* tracker layer. The strips will be read out at the far end of each leg in the L-shape; position and energy resolution measurements of the corner element will be compared against that of a single detector.

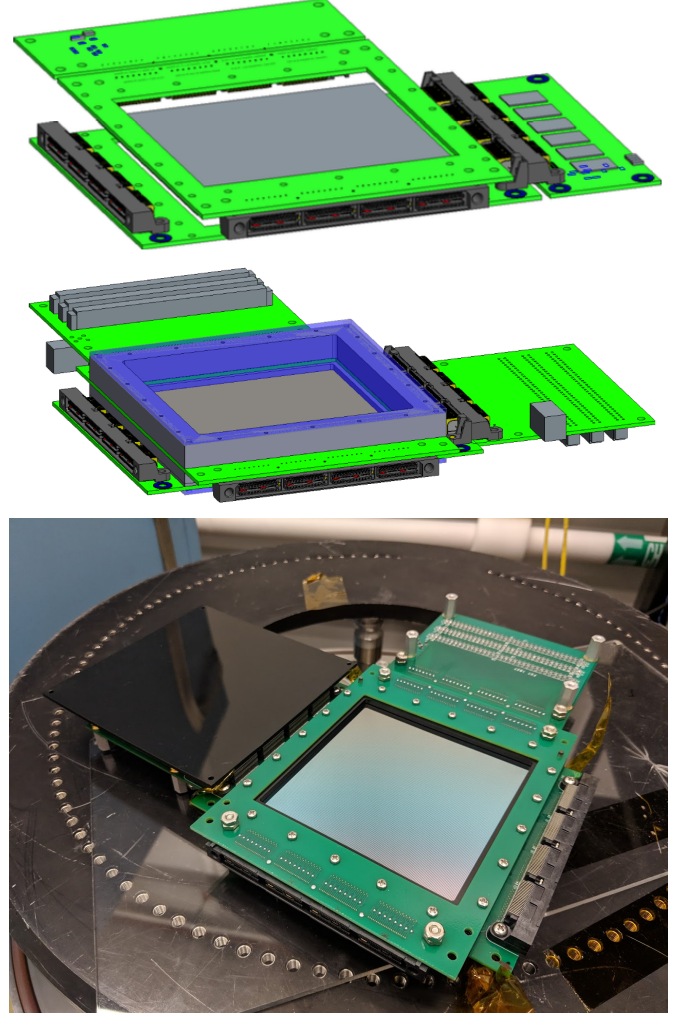


Fig. 3. **Top:** CAD model of the single-wafer carrier board printed wire boards (PWBs) with a mock-up of an ASIC readout board (right side, populated with six ASICs) mated to one of the connectors. Each carrier is made up of two of these boards with one flipped and rotated 90°. The silicon detector (gray) can be seen through the window in the carrier board. **Middle:** CAD model of the carrier including Delrin structural material; in this version a 192-pin breakout board is mated to the connectors. **Bottom:** Photo of the carrier board populated with a DSSD. The black plate normally covers the DSSD to provide some amount of light protection and to prevent accidental damage to the detector. The bottom side of a signal breakout board can be seen mated to the top-left connector.

### C. Front-End Development

The ASIC currently under consideration for the *AMEGO* tracker is the IDEAS VATA460.3 [8]. A development board containing one of these ASICs is undergoing testing at NASA Goddard to verify noise, power consumption, linearity, and maximum trigger rates. This ASIC is a highly configurable, 32-channel, combined preamplifier and 10-bit pulse-height-measuring digitizer, supporting both positive



and negative polarity input pulses<sup>1</sup>. The maximum *analog* dynamic range is  $-90\text{ fC}$  ( $+50\text{ fC}$ ) which corresponds to an energy deposition of  $\sim 2.0\text{ MeV}$  ( $1.1\text{ MeV}$ ) in silicon<sup>2</sup>. The *digital* dynamic range (*i.e.* the subset of the analog dynamic range covered by the digitizer) can be adjusted using configuration registers. The ASIC has a global trigger threshold and each channel can be fine-tuned to account for channel-to-channel differences.

The noise performance of the tracker ASIC is critical to the performance of *ComPair* and *AMEGO*, in particular at low energies where the energy of Compton scattered electrons is small. The noise in the readout electronics due to parasitic capacitance in the silicon detectors and associated interfaces scales linearly with load capacitance. It is possible to measure this behavior by loading an ASIC input with capacitors of different values and measuring the width of the fluctuations about the pedestal. For these measurements, a simple test board was made with selectable capacitor values with which to load an input channel, and the ASIC was externally triggered at  $500\text{ Hz}$  for  $240\text{ s}$  to provide sufficient statistics. The measured ADC values were binned; the mean of the distribution is the pedestal for that channel and the width (RMS) corresponds to the noise.

An example noise measurement for one channel is given in the top panel of Figure 4; each distribution is well-approximated by a Gaussian distribution. The RMS of each distribution is plotted as a function of the load capacitance in the bottom panel of Figure 4. As expected, the data are linear with load capacitance. Note that in this setup, it is only possible to measure the *slope* of this curve, since the  $x$ -axis includes only the load capacitance and not any additional capacitance due to (e.g.) traces on the ASIC circuit board between the input headers and input wire-bond pads.

While the DSSDs are being manufactured, the ASIC is being tested to read out single-sided silicon detectors already located at Goddard; these detectors have already been fully characterized so will provide a useful reference moving forward. Furthermore, this allows for software and procedures required

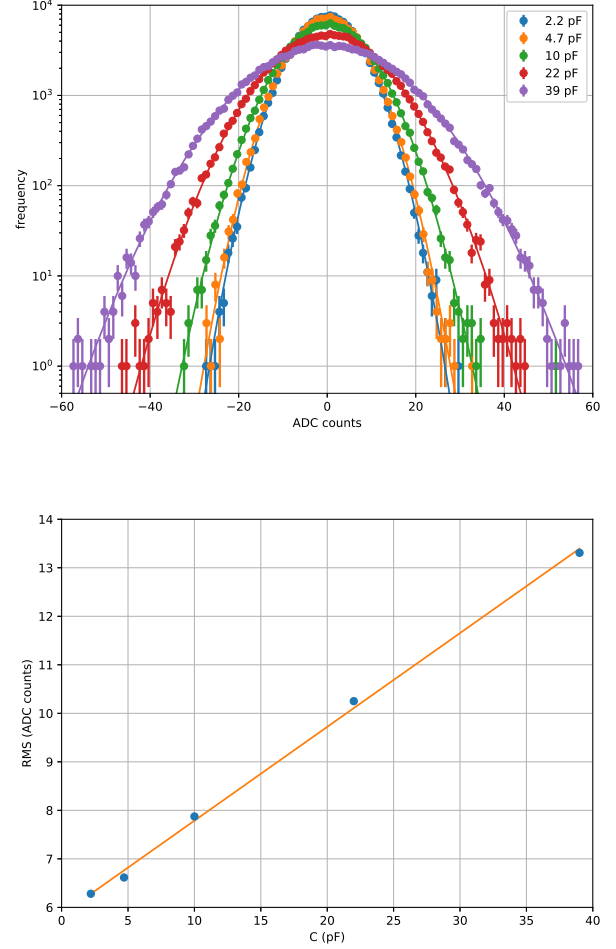


Fig. 4. **Top:** Histogram of data taken by externally triggering the ASIC while one of its inputs was under capacitive load. The mean ADC value (*i.e.* the pedestal) has been subtracted. Each distribution is well-defined by a Gaussian, also shown as a colour-coded line. **Bottom:** RMS ( $\sigma$ ) of the above histograms as a function of capacitor value. The  $x$ -axis does not include any additional capacitance due to (e.g.) the ASIC test board itself, so the  $y$ -intercept of this line is an upper limit on the noise of the ASIC.

for testing to be developed prior to the arrival of the *ComPair* silicon. A photo of the test setup is given in Figure 5. The results of the very first data measured using a  $^{137}\text{Cs}$  source are given in Figure 6. Note that these data were taken with detectors very different from the prototype detectors and hence the exact ASIC configuration used here is different from the one that will be used using the DSSDs. The noise in these measurements is also relatively high ( $\sim 11\%$  FWHM for the photo-absorption peak) due to the exact configuration used in this setup; tests of the prototype DSSDs are expected to have better performance due to lower parasitic capacitance in

<sup>1</sup>Both polarities are required, since the polarity of the pulses from the DSSDs depends on whether the signals are from strips on the ohmic or junction side of the detector.

<sup>2</sup>For positive charge, the maximum charge deposition can also be increased to  $90\text{ fC}$  albeit with reduced linearity.

the detector/ASIC interface.

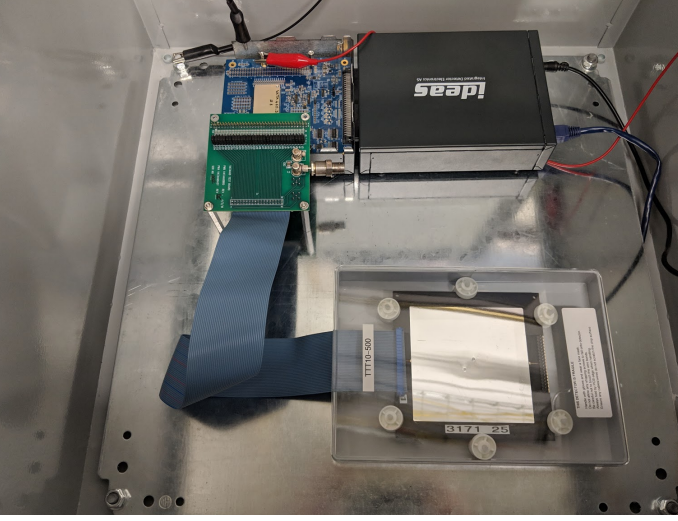


Fig. 5. Image of an IDEAS VATA460.3 development board (top right board) connected to a “Galao” readout FPGA (top right with IDEAS logo); the Galao is a universal readout board which can be used with several different IDEAS ASIC test boards which provides an Ethernet interface to the ASIC. It also includes functionality for (e.g.) external triggering and charge injection into the ASIC. The ASIC itself is contained beneath the large shield in the middle of the test board. In this setup, the ASIC inputs are connected to an interface board which, in turn, is connected to a single-sided silicon strip detector (bottom) via a ribbon cable, allowing the ASIC to digitize signals from the detector.

### III. CONCLUSIONS AND TIMELINE

*AMEGO* is a powerful MeV gamma-ray telescope that will open a window on the universe with unprecedented sensitivity. A prototype telescope is under development at NASA Goddard and the US Naval Research Lab. Over the next few months, DSSDs will arrive at Goddard and undergo testing; the associated front end electronics for the silicon subsystem are being designed in parallel. Development of a fully-custom front-end (including a custom ASIC) is also under investigation in preparation for full *AMEGO*. The other *ComPair* subsystems are also being developed; over the next year the subsystems will be integrated and beam tested in preparation for a balloon flight.

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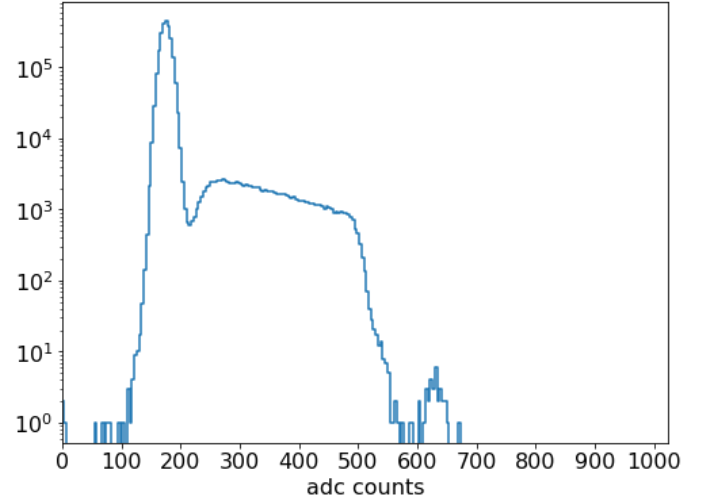


Fig. 6.  $^{137}\text{Cs}$  spectrum taken with the IDEAS ASIC and a single-sided silicon detector. The Compton edge (500 counts) and the beginnings of a photo-absorption peak (630 counts) can be seen. Fitting this peak with a Gaussian distribution yields a width of  $28 \pm 6$  counts, corresponding to a FWHM of  $\sim 11\%$ . This is relatively high due to the parasitic capacitance of this particular setup.

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